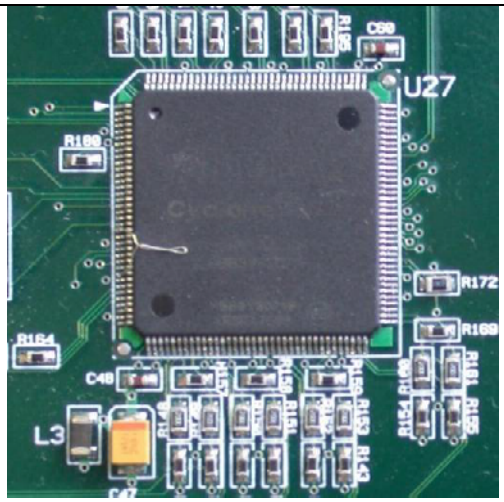
18-Channel
Wave Union TDC on FPGA

WUTDC09a

Features:

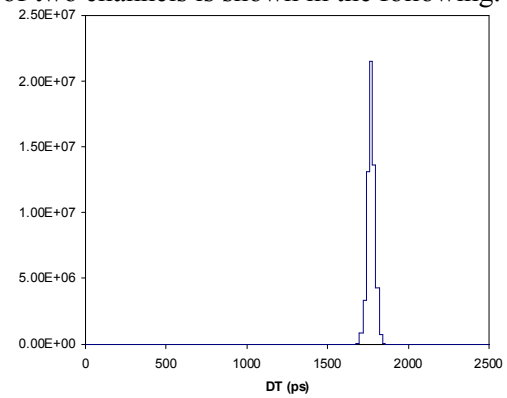
- A Wave Union TDC firmware with 18 channels implemented in an EP2C8T144C6 144-pin FPGA chip for time-of-flight applications.
- ASIC-like encapsulation to shorten learning curve for users.
- Two LVDS input banks each hosts 8 regular channels plus 1 channel for common timing reference.
- Digitizing both rising and falling edges for time-over-threshold (TOT) measurements or rising edge only for high-rate applications.
- On-chip histogram-based automatic bin-by-bin calibration for non-linearity correction and temperature compensation or optional raw data output without calibration if elected by users.
- Time measurement ΔT RMS resolution:
  - 25 ps (Rising edges).
  - 50 ps (Pulse Width).
  - 80 ps (Falling edges).
- Time measurement range: unlimited.
- Double hit separation:
  - Rising edge to next falling edge: > 7.5 ns.
  - Falling edge to next rising edge: > 7.5ns
- Continuous digitization with no dead-time nominally.
- Free running with local crystal or running with distributed system clock.
- Jam-prevention logic: < 8 hits/CH in each 2.64 μs time slice.
- Un-triggered data output via LVDS differential ports at 193.75 Mbits/s using DC balanced 8B/10B coding.



- Output capacity for 16 channels in each 5.28 μs time frame:
  - 24 hits with 1 output port.
  - 48 hits with 2 output ports.
  - 72 hits with 3 output ports.
  - 96 hits with 4 output ports.
- Common timing reference channels support:
  - Single pulse (common start/stop) mode,
  - Common burst mode with 2, 4 or 8 pulses and
  - Mean-timing mode.
- Register-setting-free for most common operations.
- RS232 serial port for control commands and display of diagnostic information.
- On-chip time difference histograms and channel hit counters.
- Data block display captured at the LVDS output ports after 8B/10B encoding.
- On-chip signals for calibration and operation evaluation.
- Outputs of selected test signal for debugging.

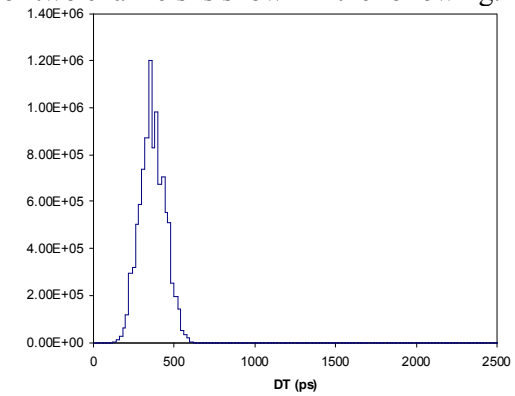
Performance

A typical rising edge time difference histogram of two channels is shown in the following:



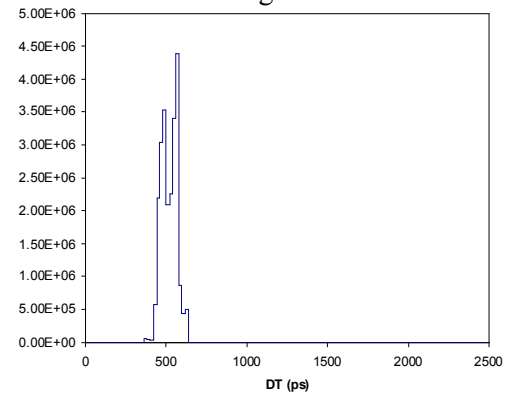
Each bin is 20.16 ps wide. The RMS resolution shown above is 24.8 ps.

A typical falling edge time difference histogram of two channels is shown in the following:



The RMS resolution shown above is 78.8 ps.

A typical pulse width variation histogram of is shown in the following:



The RMS resolution shown above is 50.4 ps.

Power Consumption

Measured power consumption of the whole chip in normal operation is 1.35 W.

Introduction

The WUTDC09a Wave Union TDC FPGA firmware is designed to perform time-to-digit conversion (TDC) in an Altera Cyclone II device EP2C8T144C6.

The chip serves 18 channels divided into two banks with 8 regular channels and 1 common timing reference channel in each bank. Typical measurement RMS resolution is 25 ps for time difference between rising edges of two channels, 80 ps between falling edges and 50 ps for pulse width (between the rising edge and the falling edge of a pulse). The target applications are time-of-flight (TOF) measurements and time-over-threshold (TOT) measurements for time walk correction or particle ID.

A feature of this design is the ASIC-like encapsulation. It is known that FPGA TDC is ultra-flexible and suitable for different user projects. However, the FPGA TDC design requires certain carefulness in various aspects beyond typical FPGA digital design practice and it may become a long learning curve for potential users. Our firmware is designed as if the FPGA is used as an ASIC TDC that provides a turn-key solution for users in a wide range of applications.

An automatic calibration functional block is provided for bin-by-bin calibration. The calibration process is performed both at the power up of the chip and during the normal operation of TDC semi-continuously. The random input hits are booked into a DNL histogram implemented with FPGA internal RAM. Each time after 4K hits are booked, the contents of the histogram are integrated and used to update the lookup table. The TDC measurements are checked through the lookup table and the center time values in picoseconds of the input bins are output. The lookup table automatically keeps track of the net effect of the temperature and the power supply voltage during the past 4K hits. The users may also dedicate certain time period to perform re-calibration process using on-chip signals.

Since the absolute time relative to the system clock is digitized for each hit, there is no limit on the range of time measurement. The encoding and post processing stages are optimized so that good double hit separation can be achieved with reasonable usage of FPGA resource. This design separates rising and falling edges as long as the time difference between them is larger than 7.5 ns.

Given such double hit separation performance, there is a risk that some hot channels can generate too large volume of data which may jam the data path in later stages. Jam prevention logic is provided in each channel to limit excessive data. During a 2.64 μs time slice, up to 8 hits from each channel are stored and extra hits are disregarded. The valid hits from all channels are then packed together for output and additional data limit is applied in this stage. Up to 24 hits from all 16 channels during a 5.28 μs time frame are packed together with a header and sent out to the first LVDS output port "cUL[0]" running at 193.75 Mbits/s using DC balanced 8B/10B coding. If there are 25 to 48 hits in a time frame, the rest of hits are output from the second LVDS ports cUL[1]. Similarly, if there are 49 to 72 hits or 73 to 96 hits in a time frame, they are output from the third or the fourth ports dUL3 or dUL4p.

The data output is an un-triggered continuous sequence with no dead-time nominally. All hits are digitized and output as long as the conditions of (1) the double hit separation, (2) the single channel hit limit in each time slice and (3) the output capacity of the entire chip are fulfilled. The scheme of the staged jam prevention is suitable for systems with high instantaneous hit rate but relatively low average rate.

This arrangement permits the users to choose appropriate output capacity to fit their specific applications. An application with low hit rate may use only one or two LVDS output ports for simplicity of the system, while a high rate application may use the full output capacity provided by all four ports.

This TDC is designed to run freely driven by a local crystal. Optionally, the users may switch

the master clock so that the device is driven by a distributed system clock. However, ultra-accurate timing for the distributed system clock is not required. The timing reference is established by using two special TDC channels, one in each input bank with 8 other regular channels.

In a special case, the timing reference system distributes a single pulse to all TDC chips. The pulse is digitized and packed into the data header. This is similar as the common start or common stop mode in conventional TDC.

Digitization precision can be improved by distributing the timing reference signals as bursts of 2, 4 or 8 pulses and using their average time as the common timing reference. The leading edge times of the pulses are digitized and averaged. The averaged time is output as the data header.

If the timing reference pulses in the bursts are distributed to travel in both directions in a cable, the common timing reference TDC channel acts as a mean timer. In the mean timing mode, the propagation delays of the cable segments linking several TDC modules and their temperature variations are compensated across all TDC modules. The mean timing scheme will be further discussed in detail in later sections.

The device operation condition can be monitored by inspecting data and histograms sent out via the RS232 port and displayed on a regular text monitor (such as HyperTerminal in many MS window based computers).

A special case of the on-chip histogram support is the channel hit counters which records total accumulated number of hits in each channel. In many applications, the hit counters are useful not only for diagnoses, but also for normal operation.

Several test signals can be output from the device for expert-level debugging.

Register-Setting-Free and Jumper-Free Operations

Full feature of the device is accessed by control and monitor the device via an on-chip RS232 serial port. However, the device can also operate stand alone without any external control support, which shortens a potential learning curve and eliminates some overhead of the system at the starting stage. Many common operating configurations can be achieved without setting registers which allows the users to use the device with minimum efforts.

When the chip is powered up, it runs an initialization sequence for about 45 seconds, during which the calibration look-up table is established. At the end of the initialization sequence, logic levels of several operation mode pins are sampled to set several internal registers which bring the device into desired operating mode. The users may tie the pins to ground or to leave them un-connected which will be weakly pulled up to high logic level by resisters inside the chip. These pins set the most essential properties of the operation: outputting time of both rising and falling edges or only rising edge; outputting raw data or calibrated data; allowing the calibration look-up table to keep updating or protect current look-up table; number of pulses in the common timing burst.

In this situation, the chip operates stand alone, free of register-setting.

On the other hand, with the support of the RS232 port. The users are allowed to set the registers inside the device for a broader range of the operation options, including overwriting configurations sampled from the mode setting pins at the end of the initialization. In this situation, the jumper setting on the board is disregarded. The device can be considered effectively jumper-free.

Pin Function Descriptions:

Pin Numbers	Mnemonic	Description
(57, 58) (71, 72) (69, 70) (64, 65) (59, 60) (47, 48) (44, 45) (42, 43) (41, 40)	TA[8](+, -) to TA[0](+, -)	The LVDS (+, -) pins of channels 8 to 0 inputs in bottom bank. Channel 8 is the common timing reference channel and channels 7 to 0 are regular channels.
(126, 125) (113, 112) (115, 114) (119, 118) (122, 121) (136, 135) (139, 137) (141, 142) (143,144)	TB[8](+, -) to TB[0](+, -)	The LVDS (+, -) pins of channels 8 to 0 inputs in top bank. Channel 8 is the common timing reference channel and channels 7 to 0 are regular channels.
(91, 90) (89, 88)	cDL[0](+, -) cDL[1](+, -)	The LVDS (+, -) input pins. The cDL[0] and cDL[1] pins are renamed inside chip as CK100A and CK100B, respectively. At least cDL[0] must be connected to a 100 MHz clock. Usually, cDL[0] is sourced by a local crystal while cDL[1] is connected to the distributed system clock.
(87, 86), 24	cDL[2](+, -) TRX1	The LVDS and single ended versions of the RS232 inputs. These two inputs are merged inside the chip. If unused, cDL[2]+ and cDL[2]- should be connected to high and low logic levels, respectively. The TRX1 can be left unconnected since it is weakly pulled up internally.
(93, 92), 25	cUL[2](+, -) TTX1	The LVDS and single ended versions of the RS232 outputs.
(101, 100) (96, 95) (76, 75) (74, 73)	cUL[0](+, -) cUL[1](+, -) dUL3p, n dUL4p, n	The LVDS outputs for data outputs. The cUL[0] and cUL[1] are enabled all the time. The dUL3 and dUL4 are tri-stated initially and can be enabled by user by setting a register inside.
28 21	CK20OUT CK20IN	These two pins are to be connected together on printed circuit board. CK20OUT is a 20 MHz clock derived from CK100A (cDL[0]). It feeds via CK20IN pin to an internal PLL to create internal clocks to generate test signals.
3	NFEdge	This is a mode setting pin to force the device to output data for rising edge only when set to high. If it is tied to ground, both rising and falling edges are output.
129	RAWONLY	This is a mode setting pin to force the device to output raw hit data only if it is set to high. When it is set to low, calibrated hit time data are output.
4	PROTLUT	This is a mode setting pin to prevent the calibration look-up table being updated during normal operation if it is set to high. If the pin is set to low, hit events during normal operation in each channel will be used to generate calibration look-up table and the look-up table will be automatically updated.
134 133 132	BURSTSZ[2] BURSTSZ[1] BURSTSZ[0]	Set expected number of pulses in each of the common timing reference burst. When this number is set to 0, 1, 3 or 7, the number of pulses to be averaged in the burst is 1, 2, 4 or 8.
30	LED	Output pin for LED.
79, 99, 9 31, 32	TP1a to TP3a VTHp, VTHn	Output pins of test signals.
Power, Ground and Configuration		The location of the power, ground and FPGA configuration pins can be found in the Altera Cyclone II device EP2C8T144C6 data sheet.
Other unused I/O		Other unused user I/O pins are reserved for future upgrade.

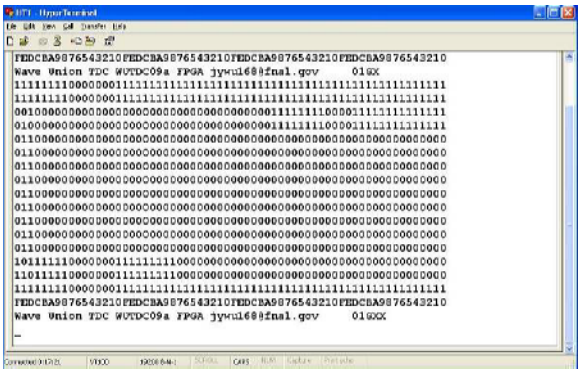
Theory of Operation

The Wave Union TDC is naturally evolved from regular delay line based TDC. In our implementation, a 60-tap carry chain in the FPGA is used as the delay line and each tap is fed to a D flip-flop existing in the FPGA logic element. The register array is driven by a 387.5 MHz (= 100 MHz x 31/8) clock generated with a phase lock loop (PLL) circuit inside FPGA.

There are two major issues in the delay chain based FPGA TDC due to uneven internal delay in the carry chain. (1) The bin widths are uneven and depend on temperature and power supply voltage, which must be calibrated as frequently as possible. (2) In many applications, the TDC resolution is limited by the "ultra-wide bins", corresponding to the carry chain crossing at the boundaries of the logic array blocks. The apparent widths of these ultra-wide bins can be several times bigger than the average bin width.

In the Wave Union TDC, hit time is encoded from the "wave union" with several 0-1 transitions rather than a single transition in regular TDC. This approach effectively subdivided the "ultra-wide bins". We have also implemented histogram based automatic calibration block for each channel. It provides a semi-continuous bin-by-bin calibration.

The following screen shot helps to explain operation of the Wave Union TDC.



In the display above, each line with 64 bits represents the bit pattern recorded in the 60-tap register array plus 4 other diagnostic signals in a clock cycle. The bit 0-3, the left-most ones are the diagnostic signals and bit 4-63 on the right are from the register array. Signals travel in the delay chain from left to right.

In the first two lines or two clock cycles, the input is low and the delay chain is in its initial condition. A bit pattern of several 0 and 1's is held in bit 4 to bit 15.

When a rising input step arrives between the second and third clock cycles, the bit pattern or the "wave union" is launched into the delay line. The snap shot of the wave union is captured by the register array at the third clock cycle as seen in the display.

A very useful implementation detail should be mentioned here. When the wave union is captured in the register array, the clock driving the register array is disabled for one (or two, occasionally) clock cycle as it can be seen that the wave union pattern stays unchanged in the fourth line in the screen. (The clock enable signal is monitored as the bit 1 shown in the screen.) By holding the wave union pattern for an additional clock cycle, the encoding process in the later stage can be implemented with fewer logic elements, which is crucial when many channels are to be fit into a low cost device.

The encoder detects the two 1-0 transitions and encodes their locations in the bit array into two 6-bit numbers. The two 6-bit numbers are summed into a 7-bit number as the raw time of the rising edge. The other 0-1 transition in the wave union is omitted for simplicity.

When the input returns to 0, the delay line recovers to its initial condition. The recovery progress is captured by the register array as shown in the third line from the bottom in the bit pattern with transition of 0-1 in the range of bit 16 to bit 63. The location of the transition is encoded as the falling edge time. Again, the register array is disabled for one additional clock cycles so that the encoding process can be implemented with fewer logic elements.

Automatic Calibration

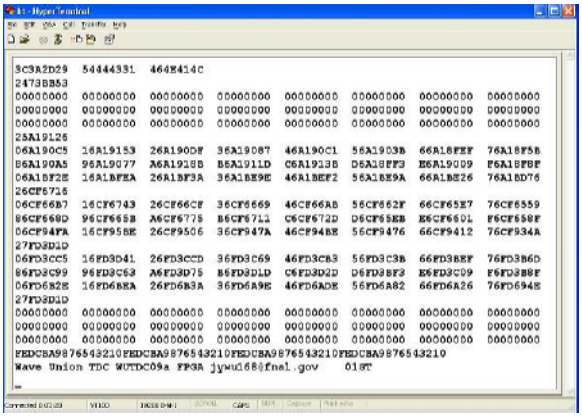
The leading edge raw time is a 7-bit number since it is a sum of two 6-bit numbers and therefore the bin widths of the wave union TDC are finer than the widths of a regular single transition TDC. The falling edge raw time is a 6-bit number in our design with coarser resolution since there is only one usable transition during the recovery of the delay chain.

Up to 8 hits during a 2.64 μs time slice from each channel are temporarily stored in the internal memory inside FPGA and extra hits are discarded to prevent the data path in the later stage from being jammed. Then the raw time data from the hits are used to generate calibration look-up tables to make bin-by-bin correction to the uneven bin widths and compensate temperature and power supply voltage variations. Each channel keeps a rising edge look-up table LUTR and a falling edge look-up table LUTF since the propagation speeds in the delay line for different logic transitions can be different. The LUTR converts the bin number of each rising edge raw time into a 9-bit fine time with least significant bit (LSB) representing 5.04 ps (1/(100 MHz x 31/8) = 2508 ps, 2508 ps/512 = 5.04 ps). The LUTF converts each falling edge raw time into a 9-bit fine time but only top 8 bits are output. So the LSB for the falling edge fine time represents 10.08 ps.

In the default operation, data for both leading and falling edges are output through the LUTR and the LUTF. The hit data are used to create new look-up tables and each look-up table is updated when a new one becomes available. The users are allowed to eliminate the falling edge data and output rising edge data only by setting the mode pin NFEdge = 1, to disable updating of the look-up tables by setting pin PROTLUT = 1 and to output raw hit data without calibration by setting RAWONLY = 1. These operation options can also be selected by setting corresponding register bits via RS232 ports, disregarding the jumper setting of these mode pins.

Output Data Format

Hit from all 16 channels are merged together and are output from the LVDS output ports in the following format.



A total of 512 bytes are output from each LVDS output port at 193.75 Mbits/s using DC balanced 8B/10B coding.

The data block header contains the first 12 bytes with the following byte definitions:

- The first byte 0x3C is the K28.1 comma code in the 8B/10B encoding table which is used to align the data block for the receiving end.
- The next 3 bytes are ASCII character strings ":-)".
- The subsequent 8 bytes are ASCII character strings "TDC1" and "FNAL" for the readout port cUL[0] or dUL3. For readout port cUL[1] and dUL4, these two strings are "Wave" and "Unio".

The users are allowed to replace these bytes with other information when the data is collected in DAQ system.

Each data block contains 5 time frames, representing a total of 5 x 5.28 μs time period. In each time frame, a 32-bit time frame header is followed by 24 hit data, also 32 bits each.

The time frame header words have the following bit definitions:

- Bit 0 to 9: Fine time with full range of 2508 ps and Bit 0 = 2.52 ps.

- Bit 10 to 19: Coarse time with full range of 2.64 μs.
- Bit 20 to 23: Readout time slice.
- Bit 24 to 31: Pulse count.

The time frame header words outputs the average of the leading edge times in a burst with 1, 2, 4 or 8 pulses. The burst summing circuit keeps a counter to count the number of pulses detected and 8 bits are output. The pulse count is used to align events across multiple TDC chips.

The hit data words have the following bit definitions:

- Bit 0, 1: If they are both 0, the data word is not a valid hit. If the hit is a rising edge, Bit 0 = 1 and Bit 1 is the LSB (= 5.04 ps) of the fine time. If the hit is a falling edge, Bit 0 = 0 and Bit 1 = 1.
- Bit 2 to 9: Fine time with full range of 2508 ps and Bit 2 = 10.08 ps.
- Bit 10 to 19: Coarse time with full range of 2.64 μs.
- Bit 20 to 27: Readout time slice. Bit 10 to 27 can be viewed as the coarse time with wider range.
- Bit 28 to 31: Channel ID.

The scales of Bit 0 to 23 are identical with the same bits in the hit data words. The bits 21 to 27 in coarse time are redundant which are provided for run time checking purpose.

The Common Timing Reference TDC Channels

Two common timing reference TDC channels are provided, one in the middle of each input bank. They have identical time measurement structure, encoder and calibration look-up table as the other regular TDC channels, sharing same temperature and power supply voltage.

Bursts of 1, 2, 4 or 8 pulses are generated by an external common timing distribution system and input to the common timing reference TDC channels of the TDC chips in the system. Only rising edges are digitized in the chip. A burst sum process block is used to process the hit data for each common timing TDC channel. The leading edge times of the pulses are averaged together as part of the time frame header. The number of pulses expected in a burst is set by the mode setting pins BURSTSZ[2..0]. When BURSTSZ = 0, 1, 3 or 7, the expected number of pulses in each burst is 1, 2, 4 or 8, respectively. This number can also be changed by setting the bits in the corresponding register via RS232 port.

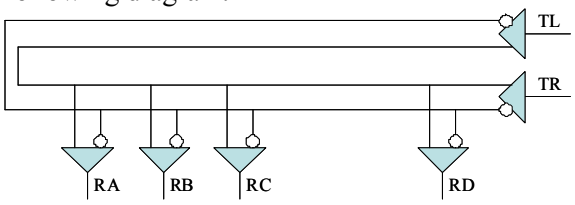
All other processes are automatically conducted. If there is no pulse in the common timing reference TDC channel for 3.3 ms (= 640K/(100 MHz * 31/16)), the burst sum block initializes all counters, including the 8-bit number of pulses counter to be included in the time frame header. When the pulses arrive, the leading edge times of the pre-defined number of pulses are accumulated. Bits are shifted downward by 0, 1, 2 or 3 steps to divide the sum by 1, 2, 4 or 8 to create the average. A starting pulse of a burst is recognized if the previous pulse is more than 645 ns (= 256 * 2.508 ns) away. Pulses with time separation less than 645 ns are considered belonging to the same burst.

The users are recommended to distribute less than a common timing burst every 5.28 μs time frame and to keep the separation of the pulses in a burst less than 320 ns to ensure correct burst summing process.

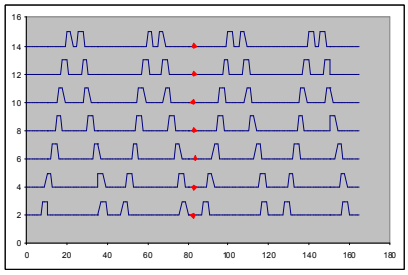
The time frame header generated by the common timing TDC channel TA[8] is sent to the output ports cUL[0] and dUL3 and the header generated by TB[8] is sent to cUL[1] and dUL4. If both common timing channels are used, at least output ports cUL[0] and cUL[1] should be used. If only cUL[0] is used, common timing reference established only by TA[8] is available.

The Mean Timing Mode of the Common Timing Reference

A very attractive timing distribution method is the mean timing scheme. The timing distribution system drives a multi-drop copper twist pair cable from both ends as shown in the following diagram.



The differential signals are received in each TDC module/FPGA and the arrival times are digitized. The mean timing burst has 8 pulses as shown in the following picture.



The left and right end drivers are alternatively enabled and drive pulses to travel from left or right end. The receivers on each TDC FPGA receive the burst with 4 pulses delayed from left path and 4 from right path. The arrival times at different TDC modules are different, but the mean times of the 8 pulses as indicated with the red dots in above are equal.

The only required condition in this scheme is that the cable segments have the same propagation delays for left-going and right-going pulses. There is no requirement on actual values of the delays and temperature variations and therefore, no requirement of using high quality media. Any moderate grade media like Cat-5 twist pair cables or even ribbon cables can serve this purpose. The TDC supports either common burst mode or mean time mode without any changes in the firmware.

The RS232 Port:

The RS232 port operates at 19200 baud, 8-bit data, 1 stop bit, no parity setting. An interface chip such as Analog Device Inc. ADM3202A is required to make voltage conversion between the FPGA and the serial port connector. Two sets of I/O pins, TRX1/TTX1 in single ended format and cDL[2]/cUL[2] in LVDS format are provided for users' convenience. The LVDS version is usually used for low noise remote control while the single ended is for local test connectors.

Control Commands:

The valid characters to control the device are numbers and upper case letters plus space. Although other characters are not likely to generate bad effect, they may cause unintended operations in other FPGA sharing the same RS232 port.

Most of the commands are single-character key press to instruct the device to output a set of characters to be displayed via RS232 port. Pressing the space bar 'SP' causes the same information being redisplayed. Pressing 'Z' will clear the histograms currently accumulated in the internal RAM.

The currently implemented control commands are shown in the following table:

HEX	ASCII	Notes
47	G	Set the register.
48-4B	H, I, J, K	Histogram 0-3
4C-4F	L, M, N, O	Histogram 0-3 with eye guide
50, 51	P, Q	Display internal raw data
52	R	LUTR Inspection, (4 channels rising edge).
53	S	LUTF Inspection, (4 channels falling edge).
54-57	T, U, V, W	Output data inspection from output ports cUL[0], cUL[1], dUL3 and dUL4.
58, 59	X, Y	Display wave union bit patterns page 0 and 1.
5A	Z	Erase histograms.

Registers:

Pressing 'G' causes a register being set. The chip supports up to 16 registers but only 7 are currently implemented. To set a register, simply enter a set of hexadecimal digits (0-9, A-F) followed by letter 'G' in the following sequence:

<parameters><register ID>G

The <register ID> is a hexadecimal number but currently only 1-7 are valid. The <parameters> is a set of 1 to 4 hexadecimal digits depending on the particular register.

The currently available registers are shown in the following table:

ID	Register Name	Affected by Pins After Power Up
1	OPCMD[3..0]	NFEdge PROTLUT RAWONLY
2	DCH[11..0]	Remains 0
3	TDCSEL[7..0]	BURSTSZ[2..0]
4	FSHIFTSEL[3..0]	Remains 0
5	CALTK[11..4]	Remains 0
6	CKCMD[3..0]	Remains 0
7	MSK[15..0]	Remains 0

The functions of the registers are explained in the following:

The register OPCMD[3..0]	
Bit	Function
0	Output raw data without calibration if set = 1. The logic level of mode setting pin RAWONLY is sampled in after power up.
1	Protect current calibration look-up tables if set =1. The logic level of mode setting pin PROTLUT is sampled in after power up.
2	Feed internal test pulses into all channels when = 0. If it is set = 1, TDC channels are fed from the hit input pins. It also disables the internal test pulse and disables outputting test signals from the test pins. After power up, this bit is set to 1.
3	Suppress the falling edge hit data and output leading edge data if set =1. The logic level of mode setting pin NFEdge is sampled in after power up.

The register DCH[11..0]	
Bit	Function
0	This bit is used only when DCH[3] = 0 and DCH[1] = 0. If DCH[0] = 0, the bin width of the histograms is 80 ps. If DCH[0] = 0, the bin width = 20 ps.
1	This bit is used only when DCH[3] = 0. If DCH[1] = 0, time difference of two adjacent channels are booked into histogram at 80 ps/bin resolution. If DCH[1] = 1, time difference of two channels are considered. The channels are given by DCH[11..8] and DCH[7..4].
2	This bit is used only when DCH[3] = 0. If DCH[2] = 0, the histograms represent time differences between two hits. If DCH[2] = 1, the histograms are distributions.
3	If DCH[3] = 0, Regular histograms are booked. If DCH[3] = 1, the histogram 3 is used as 32-bit hit counters. The rising edge hits for each of all 16 channels are booked into bins 112 to 127 and the falling edge hits are booked into bins 96 to 111.
4 to 11	DCH[11..8] (=CHA) and DCH[7..4] (=CHB) represent two channels to be considered when DCH[1]=1. In order to book valid histograms, set CHA < CHB.

The register TDCSEL[7..0]	
Bit	Function
0,1	Select or swap input channels. Set both 0 as default. See schematics for details.
2	Enable output LVDS port dUL3 if set = 1.
3	Enable output LVDS port dUL4 if set = 1.
4 to 6	Expected number of pulses in the common timing reference burst. After power up, the logic levels of mode pins BURSTSZ[2..0] are sampled into.
7	Unused.

The register FSHIFTSEL[3..0]	
Bit	Function
0	Force TDC channels 0-3 to pass data from higher channel only without loading their own data into the data path.
1	Force TDC channels 4-7 to pass data only.
2	Force TDC channels 8-11 to pass data only.
3	Force TDC channels 12-15 to pass data only.

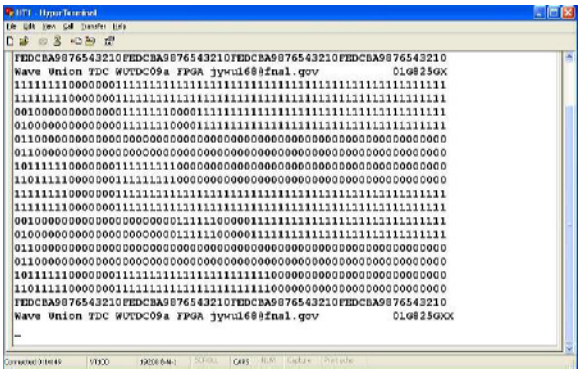
The register CALTK[11..4] The lower 4 bits CALTK[3..0] of this register is not entered. It uses the last pressed hexadecimal number.	
Bit	Function
11 & 10	=00: Output test pulses with 256 x 4 possible relative timing conditions with respect the 387.5 MHz TDC clock. Entire 2508 ps fine time range is evenly covered. =01: Output test pulses with one of the 1024 timing conditions selected by CALTK[9..0]. =1X: Output test pulses synchronized with CK100A or internal 387.5 MHz TDC clock.
	CALTK=81X: Single hit sync to 100 MHz. CALTK=82X: 2-pulse burst sync to 100 MHz. CALTK=84X: 4-pulse burst sync to 100 MHz. CALTK=88X: 8-pulse burst sync to 100 MHz.
	CALTK=9XX: Single pulse sync to 387.5 MHz, 7.524 ns wide.

The register CKCMD[3..0]	
Bit	Function
0,1	Unused.
2	Clear master timing counter TC. It may generate errors in the 8B/10B receiver in DAQ stage.
3	Switch master clock from CK100A input from cDL[0] to CK100B input from cDL[1]. It may generate errors.

The register MSK[15..0]	
Bit	Function
0 to 15	Mask each of the 16 TDC channels. =0: The channel is in normal operation. =1: The channel is masked.

Bit Pattern Display

Wave union bit pattern of TDC channel 0 can be displayed by pressing 'X', 'Y', 'Z', '[', '\', ']', '^' or '_' characters. Pressing 'X', 'Y', 'Z' etc. causes the page 0, 1, 2 etc. being displayed. The following is a screen shot of 2-pulse burst sync to 100 MHz.

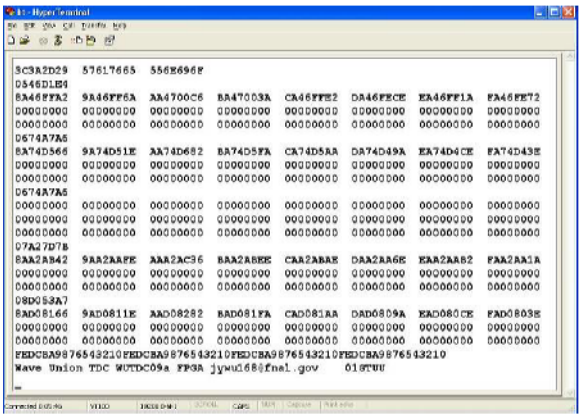


To obtain this display, press the following command sequences after the device power up: "01G" to set OPCMD to enable internal test pulse, "825G" to set CALTK to generate 2-pulse burst and "X" to see the bit pattern display.

The two pulses are both 10 ns wide and the rising edge of the second pulse is 10 ns after the falling edge of the first pulse.

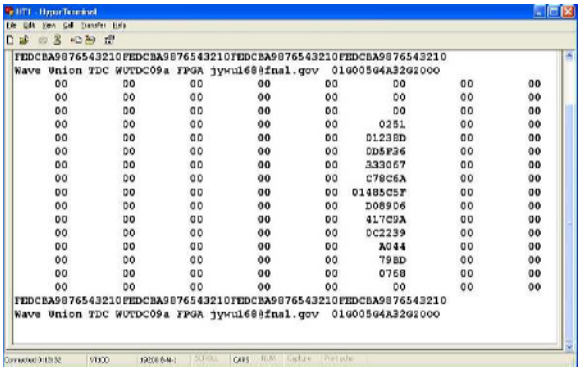
Display Output Data for Inspection

The output data from port cUL[0], cUL[1], dUL3 and dUL4 can be inspected by pressing ‘T’, ‘U’, ‘V’ and ‘W’ characters, respectively. The following is the screen shot for output cUL[1].



The Histogram Display

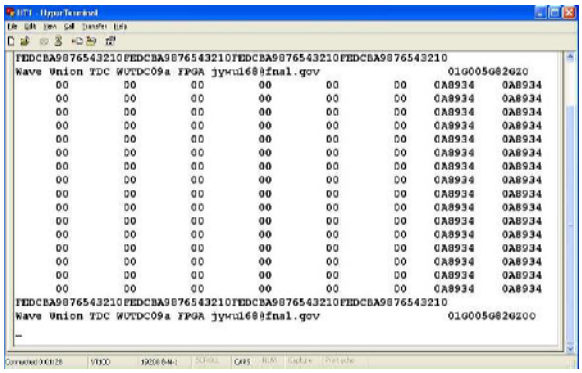
The contents of histograms 0, 1, 2 and 3 can be displayed by pressing ‘H’, ‘I’, ‘J’ and ‘K’ characters, respectively. Alternatively, these histograms can be displayed with better visual effect by pressing ‘L’, ‘M’, ‘N’ and ‘O’ characters. The following screen shot shows histogram 3 after it is booked for time difference between two channels with 20 ps/bin resolution.



The command sequences are:
“01G”
“005G”
“4A32GZO”

The Channel Hit Counters

The on-chip histograms can be used as channel hit counters. See the following:



The command sequences are:
“01G”
“005G”
“82GZO”

Hit counts for 16 channels are displayed in the last two columns, column 6 and column 7. The numbers in column 6 are falling edge counts and column 7 are rising edge counts. Pressing ‘Z’ will clear old contents and start to accumulate new counts. In this example, same test pulses are fed to all channels and therefore all channels should have same number of rising and falling edges. This is a useful test to ensure that all channels can detect both rising and falling edges correctly regardless the arrival times relative to the internal clock edges.